a) requesting an instruction stream from the memory unit and storing a plurality of instructions from said instruction stream in said prefetch buffer;

b) storing a size value in said prefetch buffer indicating the number of unissued words remaining in the prefetch buffer;

c) issuing a requested number of instructions from said memory unit and using the validity value to control an aligner that is coupled to the prefetch buffer and the memory unit to align the requested instructions;

d) depending on the number and size of instructions that are issued in the instruction cycle, adjusting the size value in said prefetch buffer;

e1) storing a validity value in said prefetch buffer indicating that said prefetch buffer contains valid data if not all instructions from said prefetch buffer have been issued;

e2) storing a validity value in said prefetch buffer indicating that the prefetch buffer contains invalid data if all instructions from said prefetch buffer have been issued;

-in case said prefetch buffer contains valid data:

f) issuing a requested number of instructions from said prefetch buffer and using the validity value and size value to control the aligner to align the requested instructions;

g) depending on the number and size of instructions that are issued in the instruction cycle, adjusting the size value in said prefetch buffer, respectively;

h) changing said validity value to indicate that the prefetch buffer contains invalid data if all instructions from said prefetch buffer have been issued.

2. (Amended) Method according to claim 1, wherein if in step f) the number of instructions stored in the prefetch buffer is less than the number of requested instructions, the issuing step includes combining instructions from said memory unit with prefetched instructions from said prefetch buffer.

3. (Amended) Method for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor comprising a first and second prefetch buffer, said method comprising the steps of:

storing first and second validity values for said first and second prefetch buffers, respectively;

storing a first size value and a second size value in said first and second prefetch buffers, indicating the number of unissued words remaining in the first and second prefetch buffers, respectively;

for each instruction cycle in which the microprocessor issues one or more instructions,

-in case both of said prefetch buffers contain invalid data:

a) requesting an instruction stream from the memory unit and storing a plurality of instructions from said instruction stream in said first prefetch buffer;

b) issuing a requested number of instructions from said memory unit and using the first and second validity values to control an aligner that is coupled to the first prefetch buffer, the second prefetch buffer and the memory unit to align the requested instructions;

c) depending on the number and size of instructions that are issued in the instruction cycle, adjusting the first size value in said first prefetch buffer,

d) setting the first validity value to indicate that said first prefetch buffer contains valid data if not all instructions from said first prefetch buffer have been issued;

e) setting the first validity value to indicate that the first prefetch buffer contains invalid data if all instructions from said first prefetch buffer have been issued;

-in case at least one said prefetch buffers contains valid data:

f) issuing a requested number of instructions from said at least one prefetch buffer and using the first and second validity values and the first and second size values to control the aligner to align the requested instructions;

g) depending on the number and size of instructions that are issued in the instruction cycle, adjusting at least one of the size values for said at least one prefetch buffer;

h) setting at least one of said validity values to indicate that said at least one prefetch buffer contains invalid data if all instructions from said at least one prefetch buffer have been issued.

4. (Amended) Method according to claim 3, wherein if in step f) the number of instructions stored in the first prefetch buffer is less than the number of requested instructions,

the issuing step includes combining instructions from the second prefetch buffer with instructions from the first prefetch buffer.

5. (Amended) Method according to claim 3, wherein before step f) the following steps are inserted:

e1) requesting an instruction stream from the memory unit and storing a plurality of instructions from said instruction stream in another prefetch buffer that contains invalid data;

e2) setting said validity value for said another prefetch buffer to indicate that said another prefetch buffer contains valid data.

6. Method according to claim 3, wherein in step g) additional information will be set in both prefetch buffers indicating which prefetch buffer contains older instructions with respect to an instruction sequence.

7. (Amended) Method according to claim 3, comprising after step f), in case of one prefetch buffer containing invalid data, the step of requesting an instruction stream from the memory unit and storing a plurality of instructions from said instruction stream in the respective other prefetch buffer.

8. (Amended) Method according to claim 3 comprising after step c) the step of requesting an instruction stream and storing a plurality of instructions from said instruction stream in the second prefetch buffer.

Please add the following claims:

14. Method according to claim 3, wherein aligning the requested instructions includes setting a plurality of multiplexers according to the first and second validity values and the first and second size values.

15. Method according to claim 3, wherein indicating the number of unissued words includes storing the number of issued words.